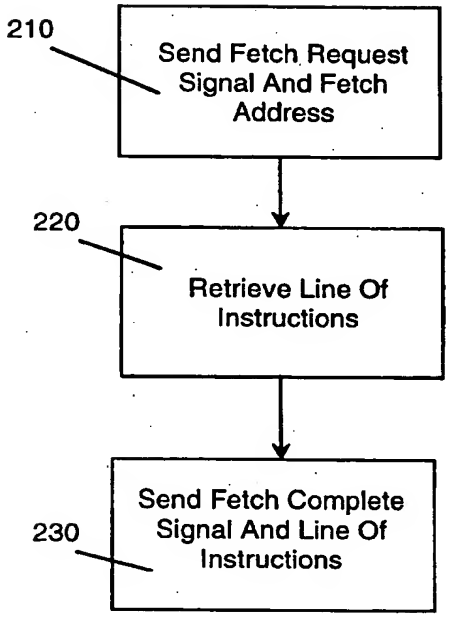
210
Send Fetch Request Signal And Fetch Address
220
Retrieve Line Of Instructions
230
Send Fetch Complete Signal And Line Of Instructions

Fig. 1

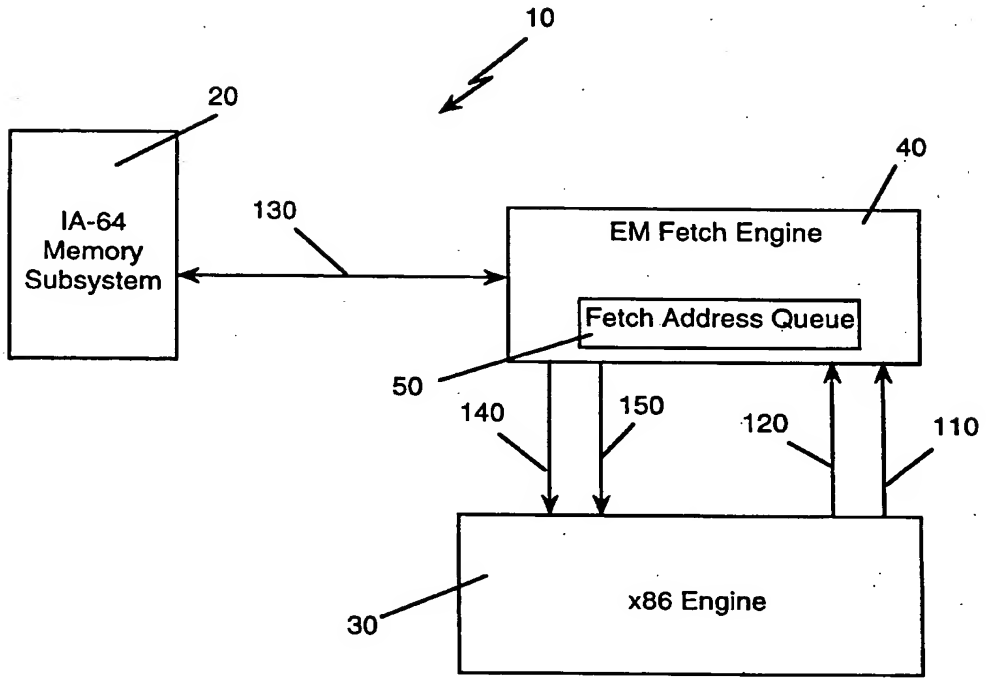
10
20
IA-64
Memory
Subsystem
130
40
EM Fetch Engine
Fetch Address Queue
50
140
150
120
110
x86 Engine
30

Fig. 2

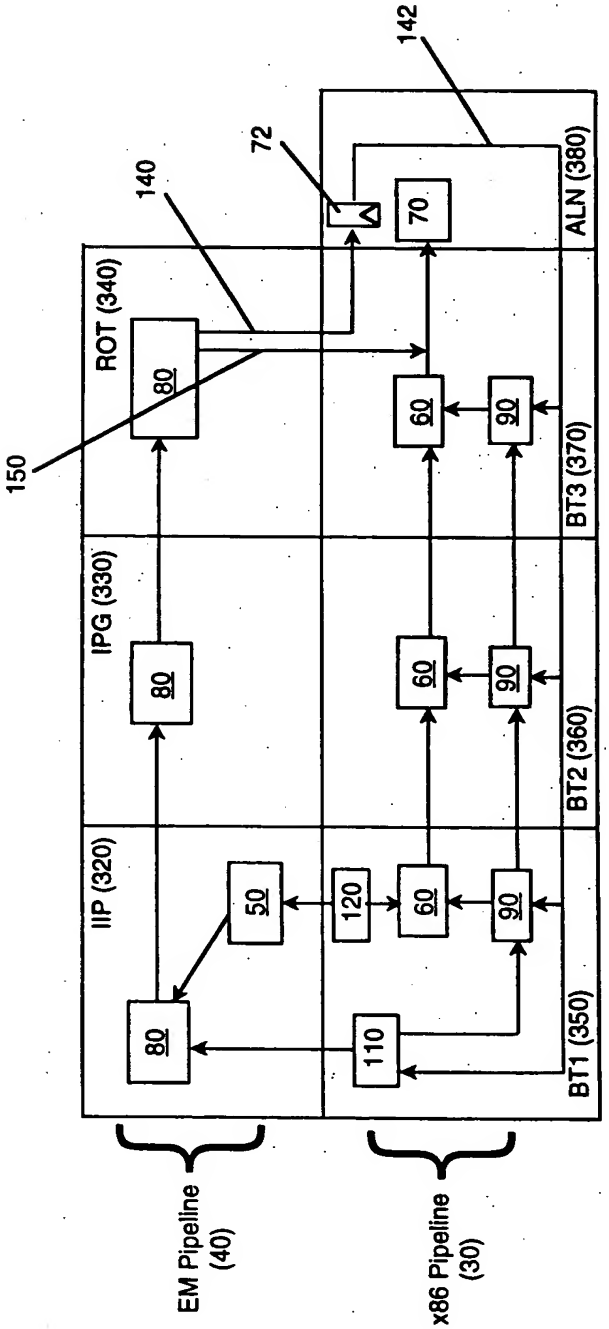
142
72
140
150
ROT (340)
IPG (330)
IIP (320)
ALN (380)
BT3 (370)
BT2 (360)
BT1 (350)
70
80
60
90
50
120
110
EM Pipeline (40)
x86 Pipeline (30)

Fig. 3

Progression of Fetch Address Through Fetch Engine (40)

		IIP (320)	IPG (330)	ROT (340)
	t	A		
	t+1	B	A	
511 -	t+2	C	B	A
512 -	t+3	D	C	B
513 -	t+4	D	C	B
	t+5	E	D	C
	t+6	F	E	D

Fig. 4a

x86 Engine Mirrored Progression of Fetch Addresses (30)

		BT1 (350)	BT2 (360)	BT3 (370)	ALN (380)
	t	A			
	t+1	B	A		
521 -	t+2	C	B	A	
522 -	t+3	D	C	B	A
523 -	t+4	D	C	B	--
524 -	t+5	E	D	C	B
	t+6	F	E	D	C

Fig. 4b

Progression of Fetch Address 120 Through Fetch Engine (40)

		IIP (320)	IPG (330)	ROT (340)
	t	A		
	t+1	B	A	
531 -	t+2	C	B	A
532 -	t+3	D	C	B
533 -	t+4	D	C	B
	t+5	E	D	C
	t+6	F	E	D

(Prior Art)

Fig. 5a

x86 Engine Mirrored Progression of Fetch Requests 120

		BT1 (350)	BT2 (360)	BT3 (370)	ALN (380)
	t	A			
	t+1	B	A		
541 -	t+2	C	B	A	
542 -	t+3	D	C	B	A
543 -	t+4	E	D	C	B
544 -	t+5	E	D	C	B
	t+6	F	E	D	C

(Prior Art)

Fig. 5b

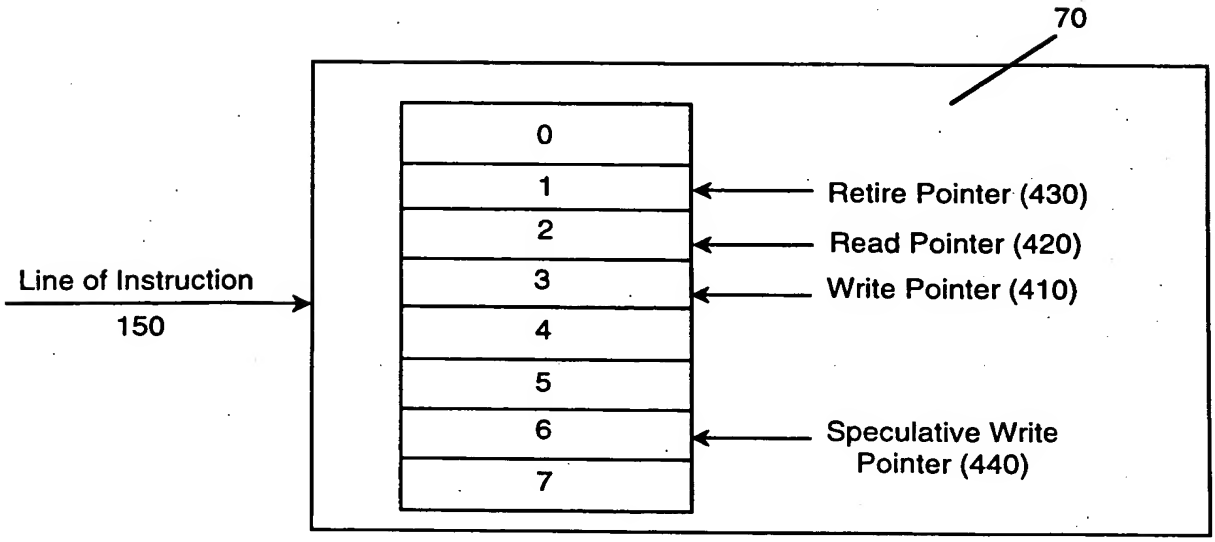
70
0
1
2
3
4
5
6
7
Retire Pointer (430)
Read Pointer (420)
Write Pointer (410)
Speculative Write Pointer (440)
Line of Instruction
150

Fig. 6